IN THE CLAIMS:

Please cancel claims 9-20 without prejudice or disclaimer and add new claims 21-32, as follows:

1. (original) A multi-threading processor, comprising:

a first instruction fetch unit and a second instruction fetch unit;

a multi-thread scheduler unit coupled to said first instruction fetch unit and said second instruction fetch unit;

an execution unit coupled to said scheduler unit, wherein said execution unit is to execute a first active thread and a second active thread; and

a register file coupled to said execution unit, wherein said register file is to switch one of said first active thread and said second active thread with a first inactive thread.

2. (previously amended) A multi-threading processor as recited in claim 1, further comprising an on deck context unit coupled to the register file, wherein said on deck context unit is to maintain the first inactive thread and a second inactive thread.

3. (previously amended) A multi-threading processor as recited in claim 2, wherein said register file is to switch one of the first active thread and the second active thread with the second inactive thread.

4. (original) A multi-threading processor as recited in claim 3, further comprising:

a first instruction decode unit coupled between the first instruction fetch unit and the scheduler unit; and

a second instruction decode unit coupled between the second instruction fetch unit and the scheduler unit.

5. (original) A multi-threading processor as recited in claim 1, wherein the scheduler unit is a four thread scheduler unit, further comprising:

a third instruction fetch unit coupled to said four thread scheduler unit; and

a fourth instruction fetch unit coupled to said four thread scheduler unit.

6. (original) A multi-threading processor as recited in claim 5, wherein said register file is a four way register file.

7. (original) A multi-threading processor as recited in claim 6, wherein said register file is to switch one of the first active thread and the second active thread with a second inactive thread.

8. (original) A multi-threading processor as recited in claim 7, further comprising:

a third instruction decode unit coupled between the third instruction fetch unit and the four thread scheduler unit; and

a fourth instruction decode unit coupled between the fourth instruction fetch unit and the four thread scheduler unit.

9-20. (canceled).

21. (new) A system, comprising:

a cache memory; and

a multi-threading processor coupled to the cache memory, the multi-threading processor comprising:

a first instruction fetch unit and a second instruction fetch unit;

a multi-thread scheduler unit coupled to said first instruction fetch unit and said second instruction fetch unit;

an execution unit coupled to said scheduler unit, wherein said execution unit is to execute a first active thread and a second active thread; and

a register file coupled to said execution unit, wherein said register file is to switch one of said first active thread and said second active thread with a first inactive thread.

22. (new) The system as recited in claim 21, wherein the multi-threading processor further comprises an on deck context unit coupled to the register file, wherein said on deck context unit is to maintain the first inactive thread and a second inactive thread.

23. (new) The system as recited in claim 22, wherein said register file is to switch one of the first active thread and the second active thread with the second inactive thread.

24. (new) The system of claim 23, wherein the multi-threading processor further comprises:

a first instruction decode unit coupled between the first instruction fetch . unit and the scheduler unit; and

a second instruction decode unit coupled between the second instruction fetch unit and the scheduler unit.

25. (new) The system as recited in claim 21, wherein the scheduler unit is a four thread scheduler unit, the multi-threading processor further comprising:

a third instruction fetch unit coupled to said four thread scheduler unit; and

a fourth instruction fetch unit coupled to said four thread scheduler unit.

26. (new) The system as recited in claim 25, wherein said register file is to switch one of the first active thread and the second active thread with a second inactive thread.

27. (new) A method, comprising:

providing a first instruction fetch unit;

providing a second instruction fetch unit;

coupling a multi-thread scheduler unit to the first instruction fetch unit and the second instruction fetch unit;

coupling an execution unit to the scheduler unit;

executing a first active thread and a second active thread with the execution unit;

coupling a register file to the execution unit; and

using the register file to switch one of the first active thread and the second active thread with a first inactive thread.

28. (new) The method as recited in claim 27, further comprising:

coupling an on deck context unit to the register file; and

using the on deck context unit to maintain the first inactive thread and a second inactive thread.

29. (new) The method as recited in claim 28, further comprising:

using the register file to switch one of the first active thread and the second active thread with the second inactive thread.

30. (new) The method as recited in claim 29, further comprising:

coupling a first instruction decode unit between the first instruction fetch unit and the scheduler unit; and

coupling a second instruction decode unit between the second instruction fetch unit and the scheduler unit.

31. (new) The method as recited in claim 27, wherein the scheduler unit is a four thread scheduler unit, further comprising:

coupling a third instruction fetch unit to the four thread scheduler unit; and

coupling a fourth instruction fetch unit to the four thread scheduler unit.

32. (new) The method as recited in claim 31, further comprising:

using the register file to switch one of the first active thread and the second active thread with a second inactive thread.